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Self-aligned ALD AlO_x T-gate insulator for gate leakage current suppression in SiN_x-passivated AlGaN/GaN HEMTs

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ABSTRACT

A proof-of-concept metal–insulator–semiconductor (MIS) AlGaN/GaN high-electron mobility transistor (HEMT) that uses a self-aligned 10 nm AlO_x gate insulator and SiN_x passivation in the device access regions was investigated. Self-alignment of the gate insulator to metal was achieved by utilizing a submicron tri-layer photoresist pattern to lift-off sequentially-deposited AlO_x dielectric and Ni/Au gate metal layers. By keeping the temperature low (100 °C) during the atomic-layer deposition (ALD) of AlO_x, reflow of the photoresist pattern was prevented, which maintained the integrity of its re-entrant profile. After lift-off, the resulting transistor gate had a T-shaped profile with AlO_x directly under the gate metal only. In a split wafer comparison, this experimental structure reduced reverse-bias gate leakage current after passivation by one to two orders of magnitude over Schottky gate devices. Plasma-enhanced chemical vapor deposition (PECVD) SiN_x passivation of the exposed AlGaN surface access regions of AlO_x-insulated gate devices was found to produce pulsed *I–V* improvements that are similar to those observed in passivated Schottky gate devices. This fabrication technique has been successfully used to demonstrate insulated gate devices with gate lengths (L_G) as short as 160 nm with $f_T = 35$ GHz and $f_{max} = 77$ GHz small-signal performance. Substantial output conductance and $f_T \cdot L_G$ product roll-off were observed at short gate lengths for both AlO_x-insulated and Schottky gate devices.

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1. Introduction

Material growth and device fabrication advancements have recently resulted in several GaN device demonstrations of high power operation at S- and X-frequency bands [1–4]. In order to push the frequency performance of GaN transistors well into the millimeter wavelength (MMW) range of 30–300 GHz, the device geometry must be scaled down in order to minimize carrier transit time. However, as lateral and vertical dimensions are reduced, increasing internal electric fields lead to excessive leakage current that limits the operational voltage range. SiN_x passivation often exacerbates this effect by raising gate leakage current and effectively lowering device breakdown voltages [5–8]. Traditional methods such as field-plates have been used in the past to distribute the peak electric fields in the device and extend the drain voltage range, but may impede MMW performance in submicron devices due to added parasitic capacitance and increased effective gate length [1,9–12]. In this study we have investigated the use of an AlO_x insulator that is deposited by atomic-layer deposition (ALD) and positioned directly under the gate metal only, to suppress gate leakage current after SiN_x passivation of the access regions. A schematic representation of this device is shown in Fig. 1a. We believe that this is the first report of a novel processing technique that uses photoresist-based lift-off of sequentially-deposited ALD AlO_x insulator and Ni/Au gate metal layers to fabricate submicron insulated T-gates for AlGaN/GaN high-electron mobility transistors (HEMTs).

Metal–insulator–semiconductor (MIS) gates have previously been shown to reduce gate leakage current and extend the operational voltage range of HEMT devices [13–15]. In addition to potential benefits that could be gained in MMW power amplifier applications, reduction of gate leakage current could also lead to lower shot noise levels [16] in GaN-based high-survivability, low-noise receiver amplifiers [17]. Large-scale integration of GaN digital logic technology based on enhancement/depletion-mode architectures [18,19] could also benefit from lower off-state gate leakage current and consequently lower static power dissipation. In each application listed above, precise control of the gate insulator thickness is required to maintain device transconductance and subsequently frequency performance. Atomic-layer deposition is a desirable growth technique to use for ultra-thin dielectric films because of its ability to grow single monolayers of material at a

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14. ABSTRACT

A proof-of-concept metal?insulator?semiconductor (MIS) AlGaN/GaN high-electron mobility transistor (HEMT) that uses a self-aligned 10 nm AlOx gate insulator and SiNx passivation in the device access regions was investigated. Self-alignment of the gate insulator to metal was achieved by utilizing a submicron tri-layer photoresist pattern to lift-off sequentially-deposited AlOx dielectric and Ni/Au gate metal layers. By keeping the temperature low (100 C) during the atomic-layer deposition (ALD) of AlOx, reflow of the photoresist pattern was prevented, which maintained the integrity of its re-entrant profile. After lift-off, the resulting transistor gate had a T-shaped profile with AlOx directly under the gate metal only. In a split wafer comparison, this experimental structure reduced reverse-bias gate leakage current after passivation by one to two orders of magnitude over Schottky gate devices. Plasma-enhanced chemical vapor deposition (PECVD) SiNx passivation of the exposed AlGaN surface access regions of AlOx-insulated gate devices was found to produce pulsed I?V improvements that are similar to those observed in passivated Schottky gate devices. This fabrication technique has been successfully used to demonstrate insulated gate devices with gate lengths (LG) as short as 160 nm with fT = 35 GHz and fmax = 77 GHz small-signal performance. Substantial output conductance and fT LG product roll-off were observed at short gate lengths for both AlOx-insulated and Schottky gate devices.

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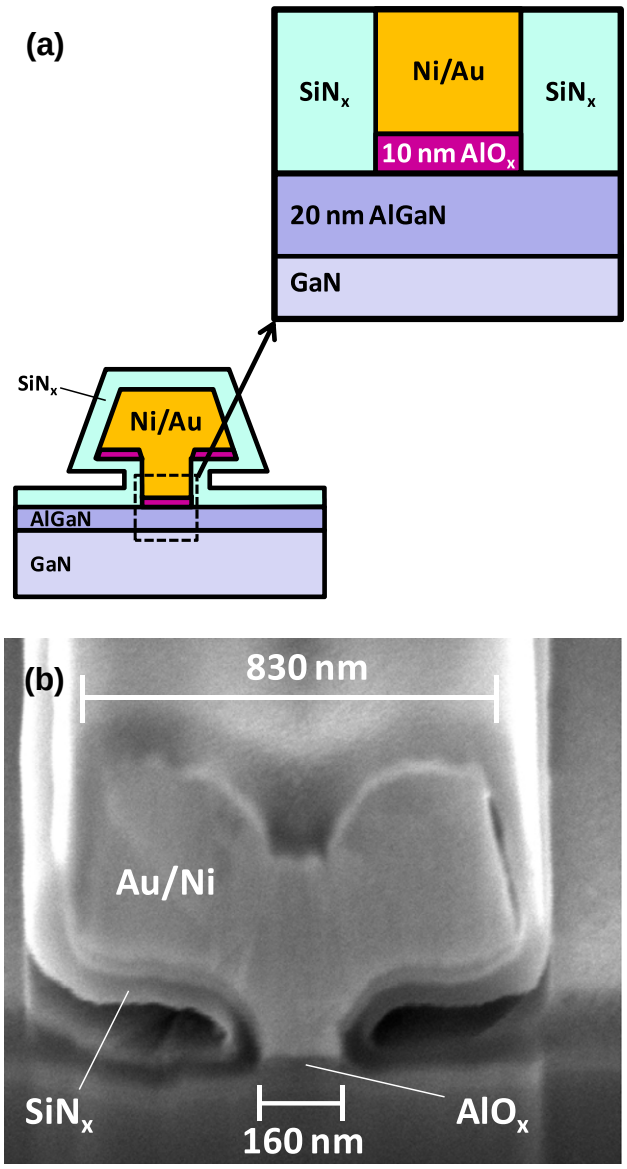

Fig. 1. (a) Schematic cross-section of self-aligned T-gate insulator/metal stack after SiN_x passivation and (b) FIB-cut, tilted cross-sectional SEM image of a self-aligned T-gate insulator/metal stack on AlGaN/GaN.

time. The specific advantage of ALD that allows for sub-nanometer-precision in film thickness is its ability to circumvent gas-phase chemical reaction limitations experienced in CVD by physically alternating pulses of gaseous precursors. This results in self-limiting surface chemical reactions only that, in certain cases, provide a large range of deposition temperatures; for example, AlO_x can be deposited by ALD from near room temperature to greater than 350 °C [20].

A conventional approach to fabricating MIS gates on HEMT devices is to pattern and define gate contacts on top of an insulator that has been blanket-deposited between the source and drain, as has been demonstrated by Ye et al. [21]. Similiarly, Saadat and co-workers have used ALD-deposited HfO_x and AlO_x as gate insulators and passivation for tungsten gate-first AlGaN/GaN HEMTs [22]. While the blanket-deposition technique produces notable DC *I–V* results, the presence of high-κ dielectric in the access regions of the device can potentially be undesirable from an RF standpoint. Kim et al. showed that when ALD AlO_x was used to passivate submicron Schottky T-gate AlGaN/GaN HEMTs, small-signal performance was degraded slightly, which was hypothesized to be due to AlO_x-related parasitic capacitance [23].

To avoid the parasitic capacitance disadvantages of a blanket high-κ dielectric process, but retain the advantages of an insulated gate and established passivation techniques, the prototype transistor described in this paper benefits from an MIS gate with 10 nm of AlO_x located directly under the gate metal only and conventional SiN_x passivation in the access regions. A split-wafer study is presented in which two samples were used to fabricate transistors that had either conventional Schottky T-gates or experimental AlO_x-insulated T-gates. The experimental T-gate AlO_x insulator and metal were self-aligned by using a tri-layer photoresist pattern to lift-off a sequentially-deposited 100 °C ALD AlO_x thin film and Ni/Au metal stack. By keeping the ALD AlO_x film deposition temperature low, reflowing of the tri-layer resist pattern was prevented and uniform lift-off was achieved. After fabrication of the MIS gate stack, conventional device passivation was achieved by plasma-enhanced chemical vapor deposition (PECVD) of SiN_x. DC *I–V*, small-signal RF, and pulsed *I–V* electrical characterization was performed in order to evaluate the conventional and experimental devices. The results of this study show that this combinatory method of gate insulation and device passivation may provide a viable technique for reducing gate leakage current in MMW frequency GaN-based HEMTs.

2. Experimental device fabrication

Heterostructure epitaxial material growth was performed by RF plasma-assisted molecular-beam epitaxy (MBE) on a 2-in. semi-insulating 4H SiC wafer. From the surface down, the device heterostructure consisted of 20 nm $Al_{0.31}Ga_{0.69}N$/1 μm undoped GaN/0.2 μm Be-doped GaN/0.1 μm AlN. Beryllium was used as a compensating dopant for residual background donor concentrations and has previously been shown to reduce interdevice isolation current in MBE-grown GaN HEMT devices [24,25]. The sheet resistance of the as-grown structure was measured using a Lehighton Electronics contactless resistivity mapper and had a value of 512 Ω/□.

Ohmic contacts were defined by standard contact lithography. After a brief Cl_2-based inductively-coupled plasma (ICP) plasma etch of the exposed AlGaN surface, e-beam evaporation of Ti/Al/Ni/Au (20/200/40/50 nm) was lifted off and annealed at 900 °C for 30 s in N_2 to achieve an average contact resistance of 0.4 Ω mm. The source–drain spacing and width of the devices used in this study were 3.5 μm and 2 × 75 μm, respectively. After ohmic contact fabrication, mesa isolation was attained through the use of a $BCl_3/Cl_2/Ar$ dry etch. Analysis of Hall Effect data showed that sheet resistance was 589 Ω/□, Hall mobility was 1310 $cm^2/V\,s$, and electron sheet density was $8 \times 10^{12}\ cm^{-2}$. After ohmic and mesa processing was completed, the split-wafer study was conducted by fabricating control Schottky T-gate devices on one sample and experimental AlO_x-insulated T-gate devices on the other.

Experimental gate fabrication of the self-aligned T-gate insulator/metal stack was carried out using the process flow that is described in Fig. 2. Conventional Schottky metal T-gates were fabricated on the control sample, using the same process flow as in Fig. 2, except with the omission of step (e): ALD deposition of AlO_x. To start off, ZEP 520A-7 was spun on each sample to an approximate thickness of 200 nm and then baked at 180 °C for 5 min. A 30 kV Raith150 electron-beam lithography system was then used to define the T-gate footprint pattern in the ZEP layer. On the experimental sample, footprint exposure doses ranged from 0.1 to 10 nC/cm resulting in gate footprint lengths (L_G) of 160–830 nm, as determined by focused ion beam (FIB) cross-sectioning and scanning-electron microscopy (SEM) measurement. In the

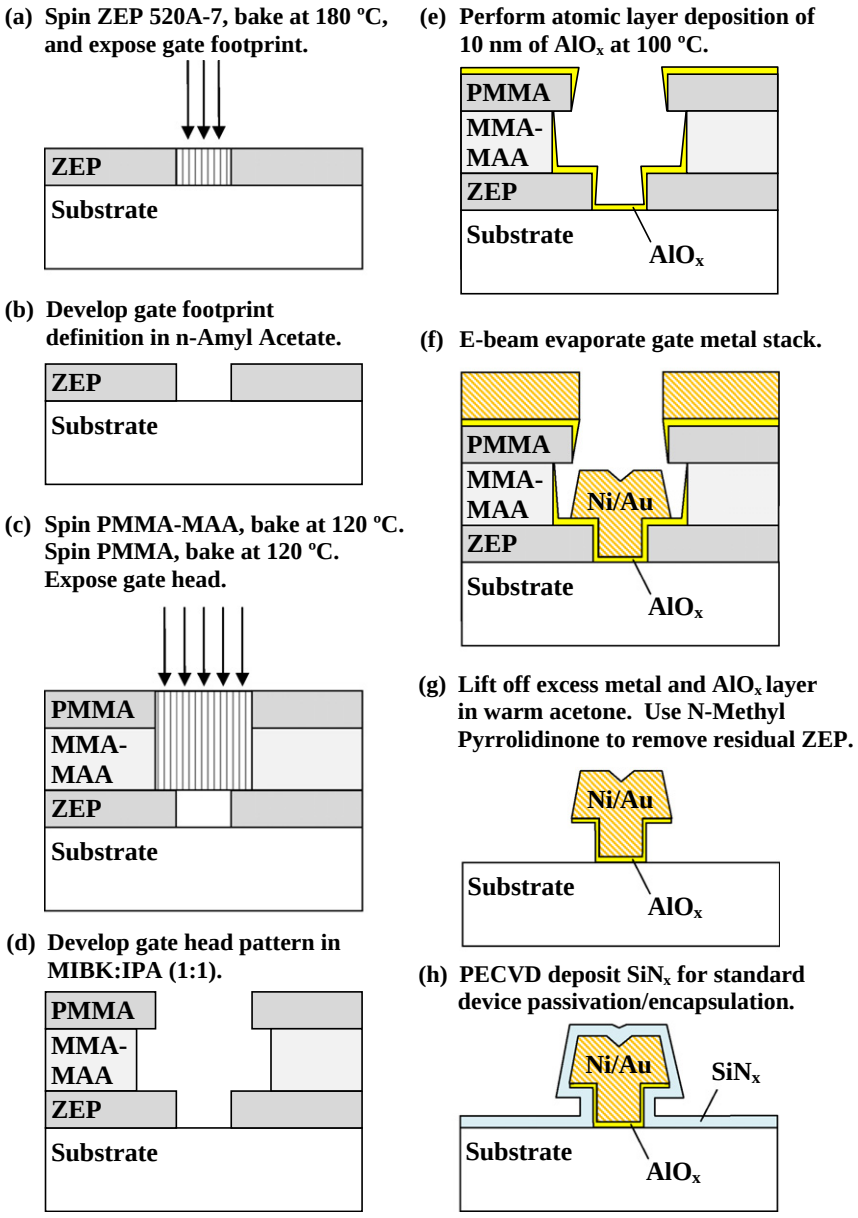

Fig. 2. Self-aligned T-gate ALD AlO_x insulator/metal stack fabrication process.

control sample, the footprint exposure doses ranged from 0.25 to 10 nC/cm, which resulted in $L_G = 90–480$ nm. After exposure, development was performed in *n*-Amyl Acetate at room temperature for 1 min and then rinsed in isopropyl alcohol (IPA). Once the footprint was defined, PMMA-MAA E9 co-polymer was spun to a thickness of approximately 400 nm and then baked at 120 °C for 2 min. Immediately after the bake, PMMA C3 was spun to a thickness of 240 nm and baked at 120 °C for 2 min. The gate head pattern was aligned and exposed using an area dose of 110 μC/cm^2. Development was then conducted in room temperature MIBK:IPA (1:1) for 2 min and then rinsed in IPA and dried. Due to its increased dose sensitivity relative to PMMA, the PMMA-MAA layer feature size increased during development causing it to undercut the PMMA. This undercutting provided the re-entrant profile necessary for lift-off, and is illustrated in step (d) of Fig. 2. After development, a 1 min low-power O_2 plasma descum was used to clean the AlGaN surface prior to insulator and metal deposition.

Once the tri-layer resist stack was patterned, a Cambridge NanoTech Savannah 200 ALD system was used to deposit a 10 nm thick AlO_x layer over the experimental sample. The reactor was preheated before sample entry to the deposition temperature of 100 °C, which was chosen to prohibit reflowing of the photoresist that occurs at temperatures above 125 °C. Upon loading, the sample was held at a pressure of 100 mTorr with 10 sccm of N_2 flowing for 10–15 min to allow for system purging and thermal stabilization. Room temperature trimethylaluminum (TMA, semiconductor purity) and triply-distilled H_2O sources were used to provide the alternating gaseous precursors for growth. Both precursors presented an approximately 1 Torr vapor pressure at room temperature. The film deposition was initiated with a single 15 ms pulse of H_2O to presumably terminate the surface with hydroxyl groups [26] before additional monolayers were grown. During AlO_x deposition, sequential 15 ms pulses of TMA and H_2O sources produced 1 Torr pressure spikes above the baseline process pressure of 200 mTorr, maintained by flowing 20 sccm of N_2. After each pulse of gas, the chamber was pumped/purged with N_2 for 8 s, allowing the system to return to baseline process pressure and removing excess precursor from the reactor and substrate surfaces.

To calibrate the growth rate per cycle, 80 nm-thick AlO_x films were deposited on Si and then measured using a monochromatic (λ = 633 nm) ellipsometer to obtain thickness and refractive index. The calibration film grown for the recipe described above had a growth rate of approximately 1.04 Å/cycle and a refractive index of n = 1.63. Based on the calibrated growth rate, 10 nm films for the experimental self-aligned T-gate insulator sample were grown employing 96 cycles. After film growth, the chamber was vented to atmospheric pressure at the growth temperature and the sample was removed.

The Schottky gate metal stack of Ni/Au (20/380 nm), used for the conventional T-gate on the control sample, was also deposited on the experimental sample immediately after ALD deposition of AlO_x using e-beam evaporation. Prior to metal deposition on the Schottky gate sample, a brief O_2 plasma descum was applied followed by a 15 s dip in $NH_4OH:H_2O$ (1:10), and then DI water rinse and dry. Both samples were lifted off in warm acetone without ultrasonic agitation, and rinsed in IPA. To remove residual ZEP photoresist, both samples were placed in a heated bath of Remover PG (N-Methyl-Pyrrolidinone-based photoresist stripper), and rinsed with IPA and DI water. After gate level processing was completed, electrical characteristics were measured across both samples before passivation.

Standard GaN HEMT surface passivation was achieved through PECVD deposition of SiN_x using an Oxford Instruments PECVD system. Prior to loading, each sample received a 2 min low-power O_2 plasma descum followed by a 15 s dip in $NH_4OH:H_2O$ (1:10), and then was rinsed in DI water and dried. After loading, the samples were held idle on the chuck under vacuum for 5 min to allow for thermal equilibration at the deposition temperature of 300 °C. During the SiN_x film growth, the pressure was held at 650 mTorr while 20 W of high frequency and 20 W of low frequency power were alternatively pulsed for 13 and 7 s, respectively in a periodic cycle. SiH_4, NH_3, and N_2 were used as gaseous precursors and were flowed into the chamber at 25, 20, and 980 sccm, respectively. To achieve the desired film thickness of 100 nm, growth time was set to 10 min. Ellipsometry measurements of films grown on Si witness test pieces showed that the refractive index of SiN_x used in this study was n = 1.96–1.97. A FIB-cut, 38°-tilted cross-sectional SEM image of the experimental self-aligned T-gate insulator/metal stack on an AlGaN/GaN device is shown in Fig. 1b. The gate footprint and head lengths of this device were measured to be 160 and 830 nm, respectively.

After SiN_x deposition, each sample was patterned for probe pad window etching and etched in a reactive-ion etching system using an SF_6-based plasma etch. Following the etch, an overlay metal stack of Ti/Pt/Au (25/25/400 nm) was e-beam evaporated to provide robust electrical probe contact. Post-passivation DC I–V, small-signal RF, and pulsed I–V electrical characterization was used to generate data for comparison of the control Schottky and experimental AlO_x-insulated devices.

3. Electrical characterization

DC I–V measurements were taken with a HP 4142 Semiconductor Parameter Analyzer and 150 μm-pitch ground–signal–ground RF probes. Drain current (I_{DS}) vs. drain voltage (V_{DS}) curves were measured beginning with a gate voltage (V_{GS}) equal to 0 V, sweeping V_{DS} from 0 V to positive voltage values and then repeating with V_{GS} steps of 1 V. I_{DS} vs. V_{GS} transfer curves were measured with V_{DS} = 5 V, and V_{GS} swept between −10 V and 5 V. Gate current (I_G) vs. V_{GS} curves were measured by sweeping V_{GS} between −10 V and 10 V, with both the drain and source grounded. Lastly, three-terminal breakdown measurements were conducted by biasing V_{GS} at 2 V below threshold voltage (V_{TH}), and sweeping the drain voltage to positive values with the source grounded. Breakdown voltage was defined as the drain voltage necessary to force 5 mA/mm of drain current (i.e. I_D = 0.75 mA for a 150 μm wide device) when the device is in this pinched-off state.

Gate-lag measurements were conducted on a custom pulsed I–V system to examine the transient response of the transistor drain current. To emulate large signal voltage swings that are present in a typical device application, a load resistor was placed in between the drain terminal and drain voltage supply. DC steady-state drain current (I_{DSS}) was first measured at V_{DS} = 20 V, V_{GS} = 0 V before the transistor was placed into an off-state quiescient bias point (QBP). At this QBP, V_{DS} = 20 V and V_{GS} was set well below V_{TH}, typically at −8 V. After holding the sample in the off-state for a few seconds, the gate voltage was pulsed from the off-state voltage to an on-state voltage of 0 V using a 0.5 μs pulse width and the drain current was measured. After applying the pulse, the gate voltage returned to the QBP. The gate-lag ratio (GLR) was taken as the ratio of pulsed I_{DS} divided by the DC I_{DSS}. Values of GLR close to unity tend to indicate that a particular device does not suffer from virtual gating and will not have trapping-impaired large signal performance [27,28].

To determine small-signal frequency performance of each sample, an Agilent E8364B PNA Series Network Analyzer was used to measure on-wafer two-port scattering parameters (S-parameters). Before device testing, short-open-load-through reference standards were used to calibrate the system. During testing, devices were typically biased at V_{DS} = 15 V, with the gate voltage biased near the point where maximum transconductance ($g_{m,max}$) was achieved in the DC I_{DS} vs. V_{GS} curve. S-parameters were measured at frequencies between 1 and 50 GHz, in 1 GHz increments. Twenty dB/decade extrapolation of the calculated hybrid parameter $|h_{21}|$ vs. frequency plot to the x-intercept at 0 dB was used to determine the unity current gain frequency (f_T). A similar extrapolation of maximum available gain (MAG) to 0 dB was used to determine each device's maximum frequency of oscillation (f_{max}).

4. Results and discussion

The primary objective of this study was to determine whether a low-temperature ALD AlO_x film, positioned directly under the gate metal would be able to suppress gate leakage current after SiN_x passivation, while also maintaining device high frequency performance. Immediate benefits of the AlO_x insulator were observed in gate I–V characteristics of SiN_x-passivated devices; a comparison between control and experimental devices with L_G = 200 nm is shown in Fig. 3. With the drain and source grounded, the AlO_x-insulated device showed a two order of magnitude reduction

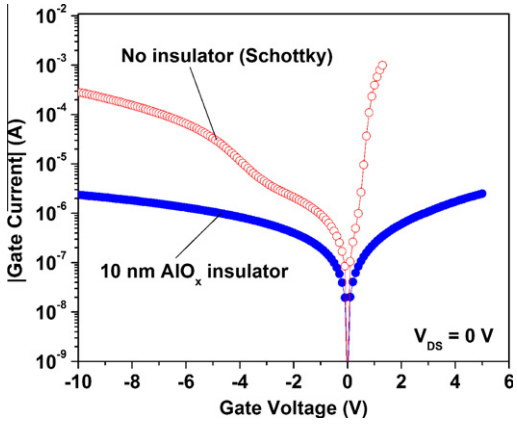

Fig. 3. Gate I–V characteristics for AlO_x-insulated and Schottky T-gate devices with L_G = 200 nm after SiN_x passivation.

in gate leakage current under reverse-bias as compared to the Schottky device. Additionally, in the positive gate voltage range, the AlO_x-insulated gate was able to be biased up to values greater than 5 V with less than 3 μA of gate current. Due to the Schottky nature of the conventional device gate electrode, forward biasing caused its gate current to exceed a compliance limit of 1 mA at $V_{GS} \geqslant 1.3$ V.

Fig. 4 shows I_{DS} vs. V_{GS} transfer curves and device transconductance for a 200 nm AlO_x-insulated gate device, after SiN_x passivation. A repeatable shift in the threshold voltage was observed when each trace was initiated with a 10-s hold time at the initial voltage and then swept in the direction indicated by the arrows in the plot. *C–V* hysteresis in ALD AlO_x capacitors has been reported previously by Saadat et al. [22] and noted to be indicative of slow trapping centers in the oxide and at the oxide/semiconductor interface [29]. Since this shift was not observed in the Schottky gate sample, this data suggests that slow charging/de-charging of traps in the AlO_x film or at the AlO_x/AlGaN interface could be occurring. Also, since a similar hysteresis was seen in *C–V* sweeps of low-temperature AlO_x MIS capacitors fabricated on Si, we suspect that this could be related to non-optimized film growth and/or improper surface preparation before oxide growth.

I_{DS} vs. V_{DS} characteristics for AlO_x-insulated and Schottky gate samples showed the presence of short-channel effects in devices with short L_G. In addition to increasingly more negative threshold voltages for smaller L_G, accentuated output conductance was evident both before and after SiN_x passivation. Typical drain characteristics for $L_G = 200$ nm and $L_G = 830$ nm AlO_x-insulated devices and $L_G = 200$ nm and $L_G = 480$ nm Schottky devices after SiN_x passivation are shown in Fig. 5. In the $L_G = 200$ nm MIS device, the increased output conductance caused incomplete pinch-off at drain voltages greater than 10 V. This increase in drain current vs. drain voltage is suspected to be due to a limited gate length to effective barrier thickness aspect ratio, L_G/t'_{bar}. The effective barrier thickness for the insulated gate stack is derived by treating the total intrinsic gate capacitance as the addition of two parallel-plate capacitors in series, and is defined as,

$$t'_{bar} = \frac{\varepsilon_{barrier}}{\varepsilon_{insulator}} \cdot t_{insulator} + t_{bar} \quad (1)$$

where t_{bar} is the semiconductor barrier thickness, $t_{insulator}$ is the physical thickness of the gate insulator, and $\varepsilon_{barrier}$ and $\varepsilon_{insulator}$ are the dielectric constants of the semiconductor barrier and the gate insulator, respectively. For the $L_G = 200$ nm AlO_x-insulated gate device, we find that the L_G/t'_{bar} ratio is approximately 7. For comparison, the $L_G = 830$ nm device has an L_G/t'_{bar} ratio of approximately

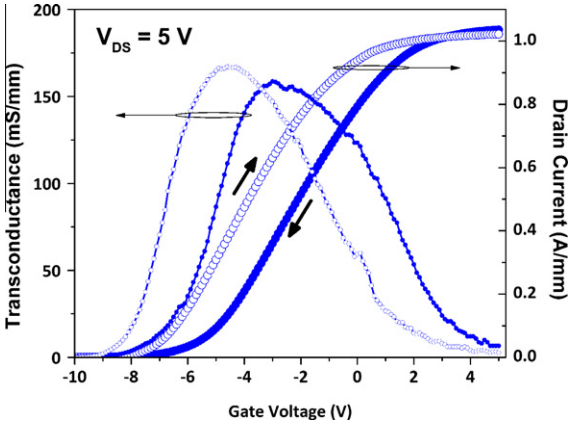

Fig. 4. Transfer characteristics of an AlO_x-insulated gate device with $L_G = 200$ nm. Repeatable hysteresis behavior was observed when the initial gate voltage was held for 10 s prior to each sweep.

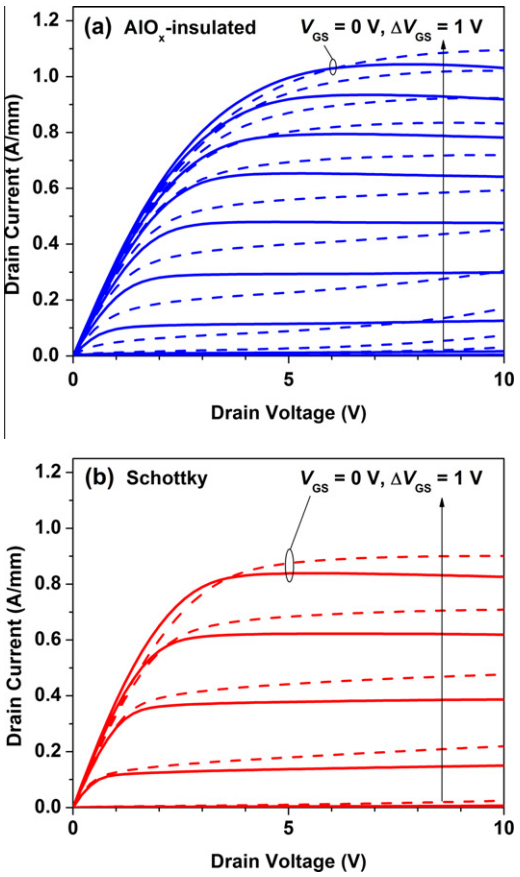

Fig. 5. Drain characteristics for (a) AlO_x-insulated gate devices with $L_G = 200$ nm (dashed blue line) and $L_G = 830$ nm (solid blue line) and (b) Schottky gate devices with $L_G = 200$ nm (dashed red line) and $L_G = 480$ nm (solid red line). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

28. Jessen and co-workers have previously observed an empirical relationship that suggests that a L_G/t_{bar} ratio of greater than 15 is required to minimize short-channel effects in AlGaN/GaN HEMTs [30]. The findings in this study are consistent with Jessen's report, and suggest that redesign of the L_G/t'_{bar} ratio is necessary to avoid output conductance in this type of MIS device.

To investigate the breakdown behavior of AlO_x-insulated and Schottky gate devices that were not affected by short-channel effects, transistors with $L_G/t'_{bar} \geqslant 24$ were examined. Fig. 6 shows a comparison between three-terminal breakdown voltage measurements of a $L_G = 830$ nm AlO_x-insulated gate device and a $L_G = 480$ nm Schottky gate device after SiN_x passivation. During this measurement, the gate of each device was biased at approximately 2 V below V_{TH}. At drain voltages less than 17 V, the AlO_x-insulated device had leakage current levels of less than 9 μA, which mirrors the drain current displayed in Fig. 6. (This leakage current includes components from both pad-to-pad interdevice isolation current and intrinsic device gate leakage current.) At $V_{DS} = 17$ V on the Schottky device, the gate leakage current was 153 μA. Despite the 15X improvement in gate leakage current for $V_{DS} < 17$ V, the device experienced an irreversible failure as gate leakage and drain currents rose rapidly once the drain voltage exceeded 17 V. Although more investigation is required, we suspect that the failure is related to breakdown of the non-optimized, low-temperature AlO_x film.

Pulsed *I–V* gate-lag measurements were performed on $L_G = 830$ nm AlO_x-insulated and $L_G = 480$ nm Schottky devices to compare the large-signal swing capability before and after SiN_x

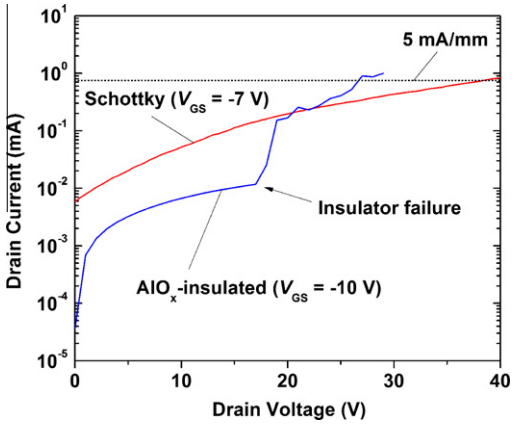

Fig. 6. Three-terminal breakdown voltage measurement comparison between L_G = 480 nm Schottky and L_G = 830 nm AlO$_x$-insulated gate devices after SiN$_x$ passivation. Gate voltage for each device is biased at approximately 2 V below threshold voltage.

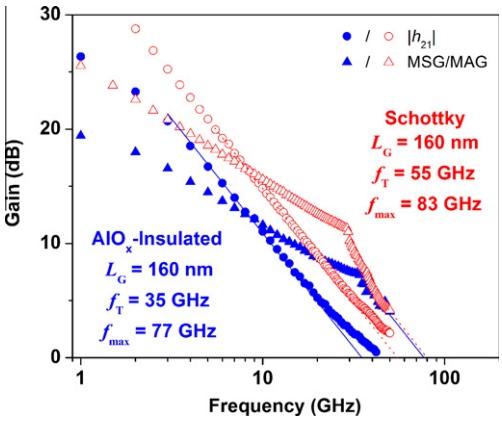

Fig. 8. Small-signal gain vs. frequency for L_G = 160 nm AlO$_x$-insulated (closed blue circles and triangles) and Schottky (open red circles and triangles) gate devices. Drain voltage is equal to 15 V and gate voltage is set for maximum DC transconductance. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

passivation. The longer gate length devices were chosen for this measurement because their lower output conductance allowed them to be taken out to 20 V drain bias under pinch-off. In general, gate length does not impact GLR results. Fig. 7 illustrates that GLR of the AlO$_x$-insulated device nearly doubled from 0.50 before passivation to 0.96 after passivation. In the Schottky device, similar improvement was seen as GLR changed from 0.22 to 0.94. This result suggests that the AlO$_x$-insulated device is capable of operating under large-signal AC excitation and that the hysteresis introduced by the AlO$_x$ does not adversely contribute to the virtual gating phenomenon seen in AlGaN/GaN HEMTs. Furthermore, the fact that virtual gating is mitigated in this type of device structure potentially provides some insight into the SiN$_x$ passivation mechanism; specifically that conduction paths, such as those provided by variable-range-hopping [31], from the gate metal to the AlGaN surface and barrier layer may not be the only avenue for charging and decharging trapping centers that contribute to virtual gating.

After measuring S-parameters and determining f_T and f_{max} as shown in Fig. 8, we have applied the same analysis that Jessen and co-workers described [30] to generate Fig. 9, a plot of $f_T \cdot L_G$ vs. L_G/t'_{bar} for various gate length conventional Schottky and AlO$_x$-insulated devices. FIB cross-sectioning and SEM measurement has been used to obtain accurate L_G values. For conventional Schottky devices t'_{bar} = 20 nm, and for AlO$_x$-insulated devices t'_{bar} = 30 nm was used. There are several implications that can be drawn from Fig. 9. First, several of the Schottky devices with $L_G/t'_{bar} < 15$ exhibit a strong $f_T \cdot L_G$ product roll-off consistent with Jessen's study. This roll-off is suspected to be related to an increased effective gate length caused by fringing gate capacitance. The second observation to note is that all of the AlO$_x$-insulated gate devices follow the *same* trend as the Schottky devices. This is important as it suggests that the AlO$_x$ film does not inherently degrade frequency response of the GaN HEMT. Instead, the insertion of the AlO$_x$ layer appears, electrically, to have the same effect as increasing the thickness of the AlGaN barrier layer. Third, if the data is re-plotted to show $(f_T \cdot t_{bar})^{-1}$ vs. L_G/t'_{bar}, the effective electron velocity ($v_{e\text{-eff}}$) limit for this material can be calculated by setting the slope equal to $2\pi/v_{e\text{-eff}}$ [30]. For the data shown on Fig. 8, the $v_{e\text{-eff}}$ limit was calculated as 1.11 × 10^7 cm/s, which is close to other reported values for GaN.

To summarize the results from this split-wafer study, Table 1 shows a side-by-side comparison of all electrical parameters generated for L_G = 200 nm AlO$_x$-insulated and Schottky T-gate devices after SiN$_x$ passivation. Please note that I_{DSS}, I_{max}, $g_{m,max}$, and V_{TH} are determined from the drain transfer characteristics with V_{DS} = 5 V. For AlO$_x$-insulated gate device data, the sweep direction of the transfer curve was from negative to positive gate voltages (off-state to on-state). Gate-lag measurements of L_G = 200 nm devices were performed at V_{GS} QBP = −10 V and a reduced drain voltage of 10 V due to output conductance limitations on drain voltage.

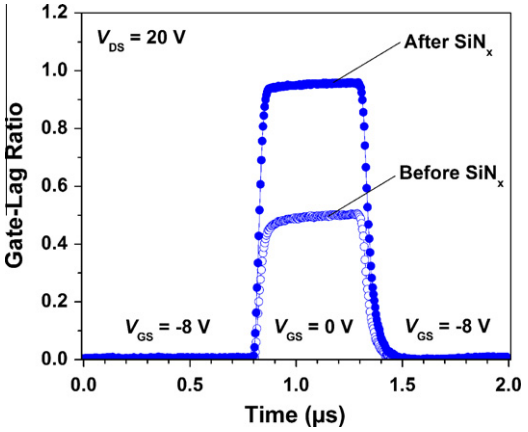

Fig. 7. Pulsed *I–V* gate-lag measurement results of an AlO$_x$-insulated gate device with L_G = 830 nm before and after SiN$_x$ passivation.

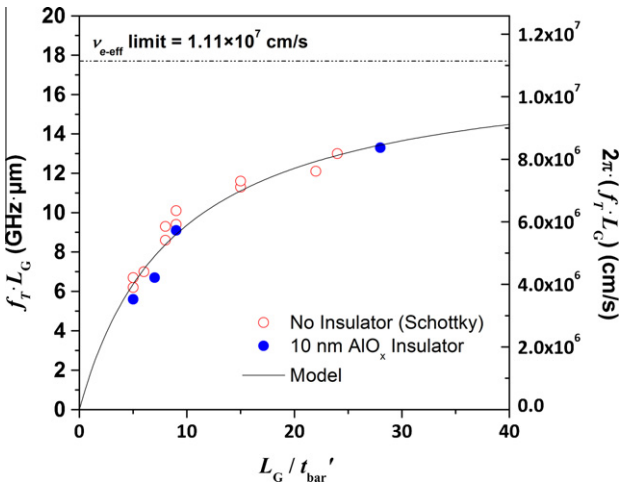

Fig. 9. Unity current gain frequency (f_T) × gate footprint length (L_G) product vs. L_G/effective barrier thickness (t'_{bar}) ratio for AlO$_x$-insulated and Schottky gate devices.

Table 1
Electrical parameters of Schottky and AlO_x-insulated gate devices with L_G = 200 nm after SiN_x passivation.

Parameter	Schottky T-gate	AlO_x-insulated T-gate
L_G (nm)	200	200
t'_{bar} (nm)	20	30
L_G/t'_{bar}	10	6.7
I_G (V_{GS} = −10 V) (A)	2.83×10^{-4}	2.38×10^{-6}
I_{DSS} (A/mm)	0.89	0.94
I_{max} (A/mm)	1.29	1.04
$g_{m,max}$ (ms/mm)	260	167
V_{TH} (V)	−4.4	−8.3
GLR	0.88	0.93
f_T (GHz)	51	32
f_{max} (GHz)	74	71
$f_T \cdot L_G$ (GHz μm)	10.2	6.4

5. Conclusions

In this study we have successfully demonstrated a proof-of-concept MIS HEMT that uses an ALD high-κ AlO_x T-gate insulator and PECVD SiN_x passivation in the access regions. This gate structure was fabricated by photoresist-based lift-off of sequentially-deposited 10 nm AlO_x film and Ni/Au metal. ALD deposition was performed at 100 °C to prevent reflowing of tri-layer photoresist patterns that allowed for uniform lift-off. To evaluate the insulator's effect on device electrical performance, a split-wafer study was conducted in order to compare experimental devices to standard Schottky T-gate HEMTs. Reverse-biased gate current after SiN_x passivation, was found to be reduced by two orders of magnitude in AlO_x-insulated gate devices as compared to conventional Schottky gate devices. Evidence of short-channel effects was observed in DC drain characteristics and $f_T \cdot L_G$ product roll-off for short gate length devices where $L_G/t'_{bar} < 15$. Drain transfer characteristics for AlO_x-insulated gate devices showed a repeatable hysteresis loop that is suspected to be related to charging/de-charging of slow trap states in the AlO_x or at the AlO_x/AlGaN interface. Despite this hysteresis, small-signal RF and pulsed I–V performance after SiN_x passivation for AlO_x-insulated gate devices were comparable to that of Schottky gate devices when increased effective barrier thickness geometry considerations were taken into account.

Further investigation into the gate breakdown failure mechanism will help provide direction for the redesign of a more robust MIS stack. Previously successful solutions for improving ALD dielectric quality, such as post-growth annealing in O_2, may provide a path to increase breakdown voltage and subsequently RF power performance. If breakdown voltage is improved, the gate-lag results suggest that this type of device could be capable of operating under large-signal conditions. Future work could be conducted to determine whether the concept of effective barrier thickness (with respect to $f_T \cdot L_G$ product) can be applied more generally to other GaN-based heterostructures, such as AlN- or InAlN-barrier HEMTs or N-polar inverted HEMTs, or to different types of dielectric insulators.

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